FD–TLM Electromagnetic Field Simulation of High-Speed Josephson Junction Digital Logic Gates

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***Abstract*— The finite-difference transmission line matrix (FD–TLM) method is extended to modeling low-T_c Josephson junction (JJ) digital logic integrated circuits (IC's), providing comprehensive simultaneous time-domain, three-dimensional (3-D) full-wave electromagnetic field and JJ device analysis. Techniques for FD–TLM modeling of a Josephson Atto-Webber switch (JAWS), a two-junction superconducting quantum interference device (SQUID), and modified variable threshold logic (MVTL) logic gates are discussed and simulation results are presented. Interconnection lengths are intentionally short so that the full-wave FD–TLM simulation results can be validated with results of conventional quasistatic-based circuit simulations. Good agreement between the simulation techniques validates the FD–TLM JJ logic circuit modeling approach. In the FD–TLM method the electromagnetic behavior of the circuit is modeled from the material properties and dimensions of the circuit, avoiding separate extractions of parasitic capacitance and inductance as needed in conventional circuit simulations.**

I. Introduction

As DIGITAL integrated circuits (IC's) such as those utilizing Josephson junctions (JJ's) [1], [2] operate at faster speeds, electromagnetic phenomena such as propagation delay, crosstalk, dispersion, and reflections must be considered to accurately model the circuit behavior. Conventional circuit analysis techniques based on modeling quasistatic parameters of parasitic inductance and capacitance, such as SPICE [3], fail at accurately modeling those circuits where the wavelength of the signals in question are comparable to the physical dimensions of the circuit. However, the full-wave finite-difference transmission line matrix (FD–TLM) method, by solving Maxwell's curl equations for the electric and magnetic fields at discrete points (nodes) in three-dimenional (3-D) space, completely models the time-evolution of electromagnetic field interaction with different media and devices [4], [5]. By selectively modifying these nodes, material properties such as permittivity, permeability, and conductance are represented. Furthermore, the FD–TLM method is capable of modeling nonlinear devices such as the JJ by altering the conductivity and permittivity of the nodes representing devices as a function of voltage and time [4], [6].

Using the FD–TLM method, a JJ IC layout is modeled by specifying the conductivity, permittivity, and permeability values at nodes contained within volumes representing substrates, conductors, and insulators. The JJ's are represented as special nodes with fixed permittivities and conductivities that change with time and applied voltage [6]. Therefore, in the FD–TLM method, only a description of the geometrical layout of the media and the devices forming a circuit need to be supplied rather than specific values for parasitic inductances and capacitances. The *fdtgraph 2.0* graphical interface program allows the user to draw the layout of a circuit on a workstation screen in a manner similar to any IC CAD system and then creates a data set in the proper format for the FD–TLM field simulator program [7]. Time required for the creation of a data set for an FD–TLM simulation is reduced from days to hours by the graphical user interface.

Josephson junctions are implemented in the FD–TLM method enabling the simulation of any type of JJ logic gate. A Josephson junction is a two-terminal device that makes use of Cooper pair tunneling and consists of a thin tunneling barrier between two superconductors [1]. In our case, we are modeling the superconductor-insulator-superconductor (S-I-S)-type Josephson junction with Nb as the superconductor and a thin layer of AlO_x insulator for the tunneling barrier.

Josephson junctions have two states, the zero-voltage state (ZVS) and the high-voltage state (HVS) [8]. While in the ZVS, the JJ behaves as a superconducting short allowing any current smaller then the critical current limit to flow with zero associated voltage drop across the junction. However, if the current through the junction exceeds its critical current, the JJ proceeds to the HVS and voltage is observed across the junction, usually approximately 2 mV. At this point the JJ behaves as a resistance R_n. Once in the HVS, the JJ exhibits a hysterisis in that it does not return to the ZVS until the current through the junction is reduced to near zero.

The ability of JJ's to switch between the LVS and HVS is used in digital logic circuits to steer current and thereby create the desired logic outputs. There are several ways to trigger the HVS in a JJ or group of JJ's. First, injecting a current through the JJ that is greater than the critical current of the JJ will cause the device to switch to the HVS. Second, applying a magnetic field of sufficient intensity to the JJ will lower its critical current, causing a steadily applied current to

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force the device into the HVS. Third, applying a magnetic field to a superconductive quantum interference device (SQUID) loop with two JJ's that are quantum mechanically coupled will reduce the total critical current for the combined JJ's. A dc bias current is usually established in this circuit so that the application of the magnetic field reduces the total critical current, causing a transition to the HVS. Finally, a combination of current injection and magnetic-field-induced critical current reduction can be used to induce the HVS as is utilized in the modified variable threshold logic (MVTL) circuit configuration. The FD–TLM method is well suited for modeling magnetic-type JJ logic circuits since magnetic fields are automatically modeled in the FD–TLM program as a consequence of currents flowing through the conductors. Thus, the performance of a circuit layout can be determined accurately from this simulation with no need for a separate inductance extraction.

In this paper, FD–TLM simulation results for Josephson Atto-Webber switch (JAWS), two-JJ DC SQUID, and MVTL logic gates having short interconnection lengths will be shown with comparison to conventional circuit simulation results using inductance values extracted from the layouts with *FastHenry* [9], an inductance calculation program. Conventional circuit simulation is performed using nodal analysis on the logic circuit with appropriate substitution of the device equations for each JJ. The nodal differential equations are then solved using an adaptive-time-step fifth-order Runge–Kutta method [10]. Since the conventional quasistatic based circuit simulation approach is suitable for modeling circuits with short interconnections, the good agreement of these simulation results with the FD–TLM simulation results validates the FD–TLM modeling approach for JJ digital logic gates.

II. FD–TLM Modeling of Jaws Logic Gates

The Josephson Atto-Webber switch (JAWS) AND gate [2] (Fig. 1) is simulated with the FD–TLM method and verified using conventional circuit simulation with important inductive parasitics extracted from the layout using *FastHenry*. This circuit contains two parasitic inductances that critically affect circuit performance at the switching speeds studied. The circuit operates by establishing a dc bias current with V_{SO}, which flows through J_2 and is less than the critical current of J_2. Since J_2 behaves as a short in the ZVS, any signal applied to the inputs (V_A or V_B) will flow through J_1 and develop additional current through J_2. If the sum of the two input currents and the biasing current through J_2 exceeds the critical current of J_2, then J_2 will switch to the HVS and behave as a resistance R_n, roughly 200 ohms. Component values are carefully selected in the JAWS AND gate so both inputs V_A and V_B must be "high" to induce switching to the HVS. After J_2 switches to the HVS, the biasing current and input currents are steered through J_1 and the small resistance R_D, at which point J_1 will also switch to the HVS, thereby steering the input currents through R_D and the biasing current through the output resistance R_{OUT}. The purpose of J_1 is to isolate the input and output currents when J_2 is in the HVS and to force current through R_{OUT}, providing a logic "high" at the gate output.

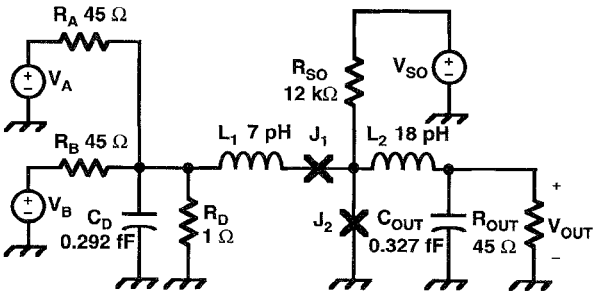

Fig. 1 Circuit diagram for the JAWS AND gate including extracted parasitic inductance and capacitance.

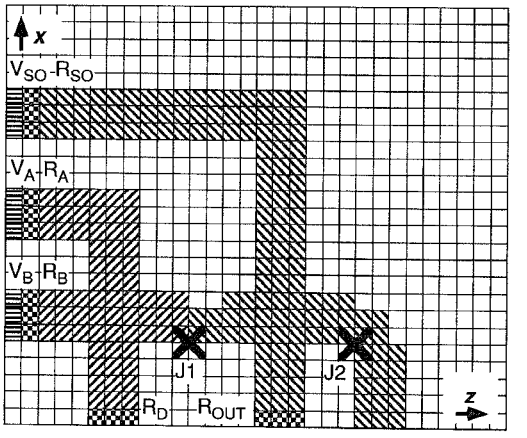

Fig. 2. Layout of the JAWS AND gate.

The JJ equations are implemented in the FD–TLM method following that of [6]. Unless noted otherwise, all JJ's in the simulations have parameters I_c = 0.1 mA, G_1 = 4.0 m℧, I_1 = 0 A, G_2 = 0.1 ℧, V_s = 2.0 mV, V_t = 0.1 mV, P_o = 3.039 × 10^{15} Wb^{-1}, and C_j = 0.5 pF, which represent the characteristics of S-I-S JJ's with AlO_x as the tunneling barrier [8]. Superconductors are implemented as perfect conductors in the FD–TLM method. Since all electromagnetic fields are assumed to be zero initially and all conductors modeled are assumed to be in the superconducting state at the beginning of the simulation, the perfect conductors will behave as superconductors having perfect conductivity and magnetic field expulsion. The circuit is simulated within a box 50 × 25 × 50 μm^3 (x, y, z) with perfectly conducting walls as boundary conditions. The circuit is placed on a 2-μm-thick layer of SiO_2 [11] with all conductors modeled as infinitely thin. Fig. 2 shows a screen-dump of the logic gate layout with a 1-μm grid spacing created with the *fdtgraph* user interface. The specifications for the JJ's, voltage sources, and resistors are supplied to *fdtgraph* as model parameters. The parasitic inductances and capacitances in Fig. 1 are not supplied to *fdtgraph* because the FD–TLM method performs a full-wave electromagnetic field simulation based on material properties and conductor geometry.

To validate the capability of the FD–TLM method to model JAWS logic gates, the circuit in Fig. 1 is also simulated using conventional circuit analysis. Kirchhoff's current law (KCL) is used to determine the nodal equations for the circuit including equations for the JJ's. Using a symbolic algebra program [12],

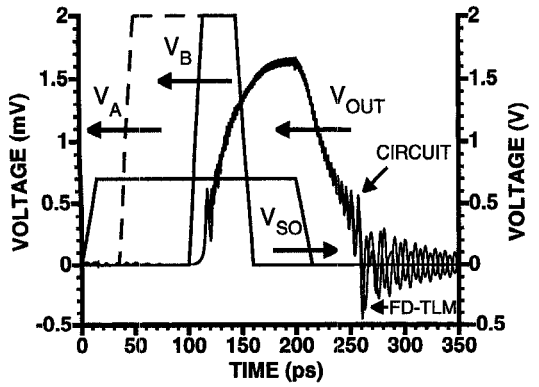

Fig. 3. FD–TLM and conventional circuit simulation results for the JAWS AND gate.

the nodal equations are solved for the first-order derivatives. The differential equations are then solved numerically using an adaptive-time-step fifth-order Runge–Kutta method [10]. The results (Fig. 3) of the FD–TLM simulation are in good agreement with the conventional circuit simulation results. To obtain correct functioning of the AND gate as shown in Fig. 3, the critical current for J_1 is set to only 70% of that for J_2 in both simulations. First, the dc biasing source V_{SO} is activated to allow switching of the gate. Then, an input voltage V_A of 2 mV is applied to the gate. As shown in Fig. 3, the logic gate does not yet produce any output signal. About 70 ps later, a 2 mV signal is also applied to V_B. After a small delay, the output of the gate V_{OUT} goes "high" verifying correct operation of the AND gate. A small oscillation is created by the JJ's in the HVS that is evident in the output voltage. After V_A and V_B are returned to 0 V, the output signal remains "high" until the biasing voltage source is returned to zero, resetting the gate.

Minor differences between conventional circuit simulation and the FD–TLM method can be attributed to accuracy of parasitic component extraction used for conventional circuit simulation. For example, all interconnections in the FD–TLM method are properly modeled as distributed components rather than lumped elements, while only pieces of the layout considered to contribute the most significant parasitic inductance were used in *FastHenry,* rather than the entire structure, leading to slightly inaccurate values for the inductance parameters. Parasitic capacitances were estimated using the parallel-plate formula, which neglected fringing effects. Several conventional circuit simulations indicate that while the parasitic inductance has a significant effect on circuit performance, the parasitic capacitance has little effect and thus the precise values of capacitance used in the simulations are not critical. Nevertheless, much effort is spent in attempting to accurately model the circuit using conventional circuit analysis, whereas the FD–TLM simulation method requires only physical circuit layout details and device parameters.

III. FD–TLM Modeling of Magnetically Coupled Josephson Logic Gates

Two-JJ DC SQUID and MVTL magnetically coupled Josephson logic (MCJL) gates, modeled using the FD–TLM method, both use magnetic coupling within a SQUID loop to trigger logic switching. A SQUID loop consists of a superconducting closed circuit with two JJ devices, J_1 and J_2, placed within the circuit as shown for DC SQUID (Fig. 4) and MVTL (Fig. 5) logic. The SQUID operates as follows. Two JJ's are coupled via the vector magnetic potential existing within the loop connecting the two JJ's or, equivalently, via the magnetic flux passing through the loop that forces a fixed phase difference between the two JJ's [1]. Quantum mechanics is used to determine the relationship between the magnetic potential and the forced phase difference between the JJ's. The gradient of the phase, $\nabla\theta$, of the pair wave function is integrated around the superconducting loop, which simplifies to the sum of the phase differences across each JJ [1]. Furthermore, the integration of the phase gradient $\nabla\theta$ around the loop must equal an integer multiple of 2π

$$\oint \nabla\theta \cdot d\ell = 2n\pi = (\theta_a - \theta_b) + (\theta_c - \theta_d) \tag{1}$$

where $\theta_a - \theta_b = \theta_1$ represents the phase change across J_1 and $\theta_c - \theta_d = \theta_2$ represents the phase change across J_2. We are left with the final relationship

$$\theta_2 = \theta_1 - \left(\frac{2\pi\Phi_e}{\Phi_o}\right) \tag{2}$$

where $\Phi_o = 2.068 \times 10^{-15}$ Wb is the flux quantum and Φ_e is the externally applied flux. Phases θ_1 and θ_2 are used in calculating the current through each JJ, e.g., for J_1

$$I_1 = I_{c1} \sin\theta_1 + G_1(V_1) + C_{j1}\frac{dV_1}{dt} \tag{3}$$

where I_1 is the current through J_1, I_{c1} is the critical current of the junction, $G_1(V_1)$ represents the current-voltage characteristics of the J_1 when in the HVS, C_{j1} is the junction capacitance, and V_1 is the voltage across J_1 [6]. The total critical current of the SQUID for any applied magnetic potential or flux can be determined using the forced phase relationship between the two JJ's. The equation

$$I_{T_c} = \text{MAX}\left[I_{c1}\sin\theta_1 + I_{c2}\sin\left(\theta_1 - \frac{2\pi\Phi_e}{\Phi_o}\right)\right] \tag{4}$$

where I_{Tc}, the maximum current that can be driven through the SQUID loop, is solved for θ_1 to give a maximum value for I_{Tc} [8]. This equation can be solved analytically for the case where both JJ's are identical and both sides of the superconducting loop are identical. However, in circuits where the JJ's are not identical or the SQUID loop is asymmetrical, numerical determination of the total critical current versus applied flux is required.

There are two methods for implementing total critical current versus applied flux in a time-domain numerical simulation method. The first method, used in [8], determines total critical current by finding the phase θ_1, which gives the maximum critical current for applied external flux Φ_e at each time step in (4). This technique provides numerical stability for large, nanosecond-size time steps even though the phase changes at a much faster rate. In the FD–TLM method, since the time step is relatively small, 1.7 fs for a 1-μm grid size, the following

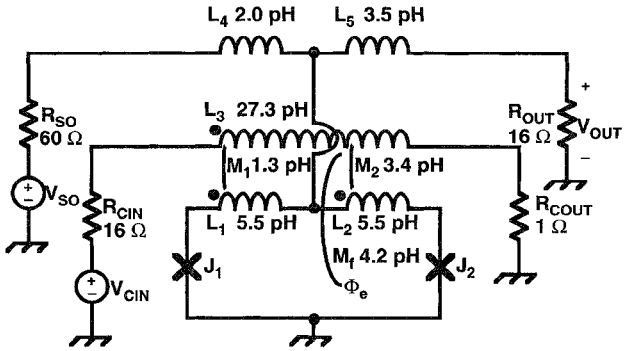

Fig. 4. Circuit diagram for the DC SQUID gate including extracted parasitic inductance.

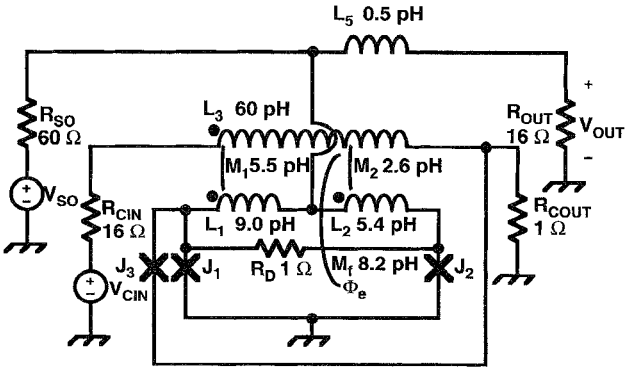

Fig. 5. Circuit diagram for the MVTL gate including extracted parasitic inductance.

method can be used. One of the JJ's is allowed to vary its phase based on the JJ equation

$$\frac{d\theta}{dt} = P_o V \tag{5}$$

where P_o is the plasma dampening frequency [1], while the second JJ has a forced phase that depends directly on the value of the phase of the first JJ and the applied flux. First, the phase of J_1 is determined by (5), which is then used to calculate the current of the JJ with (3). Equations (3) and (5) are implemented in the FD–TLM method as in [6]. Thus, within the FD–TLM simulation, the first JJ, J_1, behaves as if it is independently following the implementation of the JJ discussed in [6]. The second JJ follows the same implementation as the first JJ with the exception that (5) is not used to determine the phase for J_2. Instead, the phase for J_2 is determined from the flux in (2), where the total flux through the surface inside the loop is calculated by adding all the perpendicular H_y fields at the nodes on this surface. A three-JJ SQUID circuit [1] can easily be simulated using this method by forcing the third JJ to depend upon the second JJ in the same manner as the second depends upon the first.

To fully model the two-JJ SQUID circuit, the magnetic field created by current flowing in the loop must be considered since it will also affect the total critical current of the system. Thus, (2) is replaced by

$$\theta_2 = \theta_1 - \frac{2\pi(\Phi_e + L_2 I_2 - L_1 I_1)}{\Phi_o} \tag{6}$$

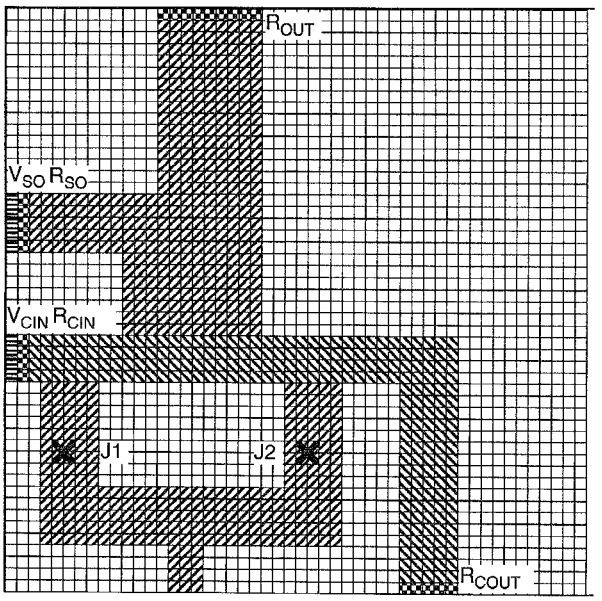

Fig. 6. Layout of the two-JJ DC SQUID.

where L_1 is the self-inductance for the side of the SQUID loop containing J_1, L_2 is the self-inductance for the side of the loop containing J_2, I_1 is the current through L_1, and I_2 is the current through L_2 [1]. However, since the FD–TLM method calculates the total flux through the surface inside the loop, it automatically includes flux created by the current flowing in these loop inductances.

A. JJ DC SQUID Logic Gate

The circuit for the two-JJ DC SQUID shown in Fig. 4 is modeled in the FD–TLM method using the layout created by the *fdtgraph* user-interface shown in Fig. 6. The circuit is modeled in a $50 \times 50 \times 50$ μm^3 (x, y, z) perfectly conducting box. The circuit is placed on a 3-μm-thick layer of SiO_2 above the ground plane with conductors 1 μm thick. The JJ parameter values are the same as those used in the JAWS circuit. Parasitic capacitance and inductance extracted from Fig. 6 are used in the conventional circuit simulation. This circuit can be operated as a multiple-input OR gate where an input V_{CIN} applied to any one of several nearby control lines triggers the gate into the HVS. However, just one control line is modeled in this example for clarity. A dc bias is first established by source V_{SO} (hence the name DC SQUID), which is less than the total critical current of the SQUID loop. When a pulse is created by V_{CIN}, the current through the control line represented by inductor L_3 in Fig. 4 creates flux within the SQUID loop. The flux lowers the total critical current of the SQUID loop causing the dc bias current to force the SQUID loop into the HVS. As a result, current from the dc-biasing source is steered through R_{OUT}, which has lower resistance than the equivalent resistance of the SQUID loop in the HVS. To return to the ZVS, the dc bias current must be reset to zero requiring the need for clocked voltage supplies for normal logic operation.

Results from the FD–TLM simulation (Fig. 7) show proper logic functioning while good agreement with conventional circuit simulation further validates the FD–TLM results. In

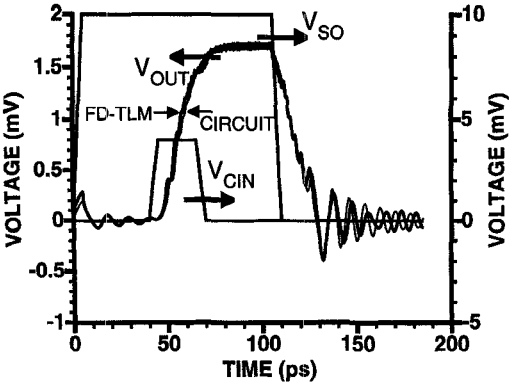

Fig. 7. FD–TLM and conventional circuit simulation results for the DC SQUID.

both simulations, a biasing voltage source V_{SO} is established to allow switching. Then, an input pulse V_{CIN} of 4 mV is applied to the control line. This signal creates flux within the SQUID loop to lower the total critical current below the value of the biasing current established by the biasing voltage source. At this point, the output voltage V_{OUT} goes to the logic "high" value and remains there until the gate is reset by setting V_{SO} to zero. Minor differences in results are caused by inexact extraction of parasitics used in the conventional circuit simulation. Parasitic capacitances had an insignificant effect on the conventional circuit simulation results as they are very small compared with the capacitance of the JJ's and thus were omitted from the conventional circuit simulation in Fig. 7. However, the parasitic inductances had a significant effect on simulation results.

B. MVTL Logic Gate

The MVTL logic gate circuit shown in Fig. 5 is modeled in the FD–TLM method using the layout shown in Fig. 8. The circuit is placed within a 50 × 50 × 50 μm^3 (x, y, z) perfectly conducting box and is located on a 3-μm-thick layer of SiO_2 above the ground plane with all conductors 1 μm thick. The JJ's are modeled using the same parameter values as before, except for J_2 having three times the critical current of J_1 and J_3. As a result of the differences in critical current for J_1 and J_2, the values for L_1 and L_2 are chosen to keep the expression $L_2I_2 - L_1I_1$, from (6), near zero. With L_1 and L_2 designed properly, self-induced flux is minimized and only current through the control line will generate flux necessary for transition to the "high" logic state.

The MVTL circuit utilizes both magnetic coupling and current injection to force the gate into the logic "high" state. As shown in Fig. 5, the current through the control line creates flux in the SQUID loop to reduce the critical current of the system as in the two-JJ DC SQUID while, in addition, the same current is also injected into the SQUID through J_3 forcing a more rapid transition to the HVS. Although only one control line is shown, a multiple-input OR gate can be constructed by connecting extra input resistors to the left end of L_3. J_3 serves as a buffer to isolate the control line current from the load and the SQUID loop when J_1 and J_2 are in the HVS. Once in the HVS, the dc bias source current is directed through

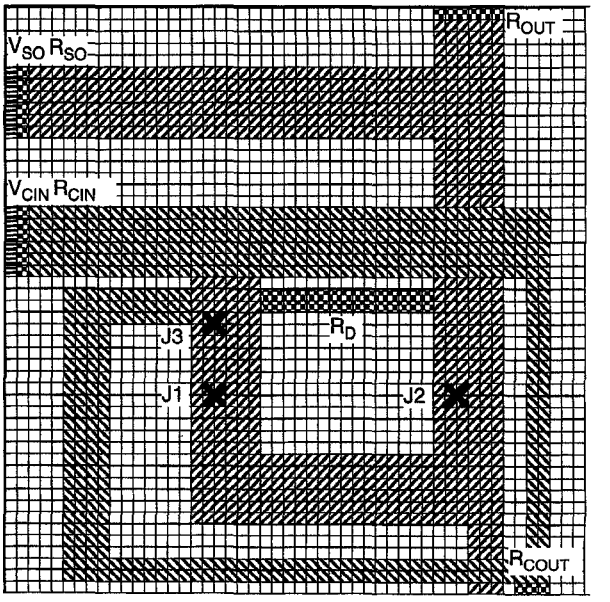

Fig. 8. Layout of the MVTL gate.

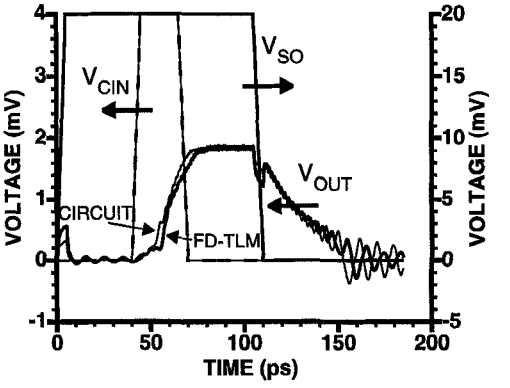

Fig. 9. FD–TLM and conventional circuit simulation results for the MVTL gate.

inductor L_5 and the output resistance. The MVTL circuit is currently capable of switching much more quickly than any of the other Josephson logic gates [2]. Switching times as low as 2.5 ps have been reported using 1.5-μm Nb/AlO_x/Nb JJ's [2]. As with the other logic gates, the circuit does not return to the ZVS after having been triggered until the power supply is switched off, thus necessitating a clocked power supply for practical logic circuits.

Conventional circuit simulation including the extracted parasitic inductance and capacitance is performed with the fifth-order Runge–Kutta method, and good agreement is obtained with the FD–TLM results as shown in Fig. 9. This gate is driven in the same manner as the two-JJ DC SQUID logic gate. Discrepancies in Fig. 9 are caused by the slightly inaccurate inductances values used in the conventional circuit simulation not completely modeling the distributed parasitics that are modeled in the FD–TLM method.

IV. Conclusion

Both resistively and magnetically coupled Josephson junction logic gates have been successfully implemented within

the FD–TLM field simulation method. Furthermore, with only the layout of the integrated circuit and the JJ parameters supplied, the FD–TLM method performs a rigorous, full-wave simulation including distributed parasitics within the system that would otherwise require tedious extraction for proper modeling in a conventional circuit simulation. Significantly, the layouts for the simulations were carefully designed so that the interconnection lengths were short, enabling FD–TLM simulation results to be validated with conventional quasistatic-based circuit simulation results. In circuits where the structural dimensions are comparable to the wavelength of signals, conventional circuit simulation techniques will be inaccurate compared with the FD–TLM approach.

Because of the generalized nature of the FD–TLM method, any type of JJ logic circuit can be simulated in both the JAWS and MCJL configurations. For example, a SQUID circuit containing ten JJ's can be modeled as easily as the two-JJ DC SQUID, whereas extra modeling effort is required using most other simulation methods. By extracting the process parameters for the JJ and then implementing these in the FD–TLM method, JJ circuits and their behavior can be fully simulated before actual circuit fabrication, reducing the costly trial-and-error effort in producing JJ logic circuits. Future FD–TLM modeling research includes implementation of superconductor-normal metal-superconductor (S-N-S) layered JJ's and grain-boundary JJ's [2], simulation of three and four JJ DC SQUID circuits [1], inclusion of high-frequency effects and penetration depths within the superconductors, and simulation of the RF SQUID [2].

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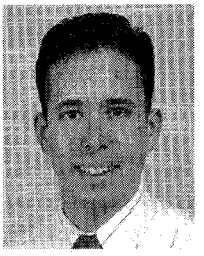

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